REMARKS

Reconsideration of the application is requested.

Claims 1-8 remain in the application. Claims 1-8 are subject to examination. Claims 1 and 5 have been amended.

Under the heading "Claim Rejections - 35 USC § 102" on pages 2-4 of the above-identified Office Action, claims 1-8 have been rejected as being fully anticipated by U.S. Patent No. 6,198,667 to Joo (hereinafter Joo) under 35 U.S.C. § 102.

The invention of the instant application relates to a test system for testing two, separate independent memory circuits in parallel. The two memory circuits are connected to the tester unit such that a circuit selection signal is connected to the first memory circuit in an inverted form and to the second memory circuit in a non-inverted form. Thereby, the tester unit can select which memory circuit is to be tested simply by setting the circuit selection signal to a specific logical value. Since the circuit selection signal only controls the acceptance of the test signals into the memory module, once a test sequence has started within a memory module, a change in the circuit selection signal does not affect the initiated test sequence.

In contrast, Joo relates to a single memory apparatus having a

multi-bank memory array and wherein an input/output for inputting and outputting data is disclosed. Therein, a separate test system is not disclosed. Rather, the tester is fully integrated onto the same semiconductor chip as are the plurality of memory banks.

In contrast, in the instant application, it is clear that the memory circuits are separate memory modules which are connectable to the tester unit so that the tester unit can carry out a test procedure on two of the memory modules simultaneously. Claims 1 and 5 of the instant application have been amended to emphasize this difference between the invention of the instant application and the invention disclosed in Joo.

Claim 1 has been amended such that it is clear that the tester, the first memory circuit and the second memory circuit are not all formed on a single integrated circuit as taught in Joo but are all separate units wherein the first and second circuits are releasably connected to the tester unit for testing.

Claim 5 has been similarly amended such that it is clear that the method is performed by a tester unit with a first and a second memory module which are distinct devices and not located within a single memory device. Support for the

changes is shown in Fig. 3 and discussed on page 17, lines 5-9 of the specification of the instant application.

Furthermore, it is noted that Joo does not appear to teach a test data generation circuit disposed on the memory chip as recited in claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 5.

In view of the foregoing, reconsideration and allowance of claims 1-8 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner Greenberg Stemer, LLP, No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner

Greenberg Stemer, LLP, No. 12-1099.

Respectfully submitted,

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